IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Carlos A. Gonzalez et al.	Examiner:	James M. Mitchell
Serial No.:	10/003,238	Group Art Unit:	2827
Filed:	October 26, 2001	Docket No.:	884.535US1
Title:	ELECTRONIC ASSEMBLIES WITH FILLED NO-FLOW UNDERFILL		
Assignee:	Intel Corporation	Customer No.:	21186

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.131 prior to any final rejection of U. S. Patent Application Serial Number 10/003,238 to establish invention of the subject matter of the rejected claims prior to January 4, 2001.

I, Song-Hua Shi, do hereby declare:

1. I have been employed by Intel Corporation from prior to January 4, 2001 until the present. My current job title is Senior Engineer.

2. I am a co-inventor of the inventive subject matter of the present application as described, illustrated, and claimed therein.

3. Prior to January 4, 2001, the inventive subject matter that is described, illustrated, and claimed in corresponding claims of the present application was completed in the United States as evidenced by the following:

   a. Prior to January 4, 2001, having earlier conceived the claimed subject matter in the United States with the co-inventors, I personally generated a draft of an Invention Disclosure, a copy of which is attached hereto as Exhibit A (8 pages). The dates that have been deleted from Paragraphs 13 and 16 of Exhibit A are prior to January 4, 2001. Other sensitive information has been blocked out from Exhibit A.

b. Figure 2 of Exhibit A illustrates conceptually an IC (integrated circuit) die having terminals being attached to corresponding pads of a substrate.

A liquid, low CTE (coefficient of thermal expansion) fluxing no-flow underfill material is dispensed on a component-mounting area of a substrate, including on the substrate pads. Particles of silica filler are shown surrounding one of the substrate pads. This is seen in the illustration in the left-hand side of Figure 2 of Exhibit A, which corresponds to FIG. 5 of the present application.

Following the direction indicated by the first arrow of Figure 2, the next illustration shows an IC with its terminals aligned with and compressed down upon the pads of a substrate, squeezing out particles from between the terminals and the pads. This illustration corresponds to FIG. 6 of the present application. As further described in Exhibit A, e.g. in Paragraph 14, in an embodiment the fluxing capability of the underfill material effectively removes metal oxide from the surface of the interconnect structure, such as terminals, pads, pre-solders, and copper materials, during a soaking period at a temperature ranging from 130-180C.

Following the direction indicated by the second arrow of Figure 2, the next illustration shows the IC with its terminals completely joined to the pads of a substrate, following the application of suitable heat to reflow solder. When cooled, the hardened underfill encapsulates the terminals, pads, and solder connections. This illustration corresponds to FIG. 7 of the present application.

It should be noted that, although Figure 2 of Exhibit A appears to show most if not all particles squeezed out from between the IC terminals and the substrate pads, in some embodiments of the IC package (such as that described below regarding Exhibit C), not all particles are squeezed out, but enough particles are squeezed out so the remaining ones do not prevent adequate physical and electrial contact between the terminals and pads after the solder reflow operation.

c. Prior to January 4, 2001, I was personally involved in the construction of prototype IC packages utilizing low CTE fluxing no-flow underfill materials, as described in Exhibit A. My responsibilities included the selection of materials and equipment; defining high-

volume, cost-effective processes to improve yield and reliability of IC-to-substrate interconnections using low CTE fluxing no-flow underfill materials; the building and testing of prototypes; and analyzing test results.

d. Exhibit B (1 page) shows an optical microphotograph of a cross-section of a prior art IC-to-substrate interconnection. I received and analyzed this microphotograph prior to January 4, 2001. This interconnection has an underfill material that did not contain any significant amount of low CTE silica particles, and in which compression was not used to press the IC onto the substrate prior to or concurrently with heating. The die is shown in the upper portion of Exhibit B. In this test, the die has a number of relatively high melting point terminals or bumps of hemispherical shape. The substrate, in the lower portion of Exhibit B, has a number of substrate pads, each of which has a relatively low melting point solder bump of roughly hemispherical shape. After subjecting this interconnection to reflow temperature, without added compression, the substrate solder bumps melted, but they did not experience adequate wetting or form good quality solder joints with the corresponding die bumps. A typical example of a poor quality solder joint with poor wetting is shown in the white-outlined box labeled "2 Solder Bumps With Poor Wetting".

e. Exhibit C (1 page) shows an optical microphotograph of a cross-section of an IC-to-substrate interconnection, in accordance with an embodiment of the present application. I received and analyzed this microphotograph prior to January 4, 2001. This interconnection has an underfill material containing low CTE silica particles, which may be seen within the underfill material in the spaces on either side of the solder joint, as well as embedded between the die terminal and the substrate pad. The silica particles were approximately spherical and ranged in size from approximately 0.1μm to 40.0 μm, with an average size of about 10.0 μm. The fluxing agent used in the underfill was ester acid, which is an organic carboxylic acid.

In addition, compression was provided by a thermocompression bonder to press the IC onto the substrate after the IC reached soaking temperature, in order to squeeze out most, but not all, of the silica particles. A cluster of silica particles may be seen in the central

portion of the solder joint.

The die is shown in the upper portion of Exhibit C. In this embodiment, prior to reflow temperature, the die had a number of relatively high melting point terminals or bumps of hemispherical shape, and the substrate, seen in the lower portion of Exhibit C, had a number of substrate pads, each of which had a relatively low melting point solder bump of roughly hemispherical shape. After subjecting this interconnection to reflow temperature, while continuing to maintain compression with the thermocompression bonder, the substrate solder bumps melted, experienced good wetting, and formed high quality solder joints with the corresponding die bumps. A typical example of a high quality solder joint with good wetting is labeled "Solder Joint".

f. When I finished testing and evaluating the prototype IC package of the type shown in Exhibit C, I believed that it worked satisfactorily for its intended purpose, by providing a potentially high yield, high reliability component package having a filled, no-flow underfill.

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 02/09/2007

Song-Hua Shi

CARLOS A. GONZALEZ ET AL.

By their Representatives,
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Date Feb. 9, 2007

By

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